Bang-Sup Song

System-level Techniques for Analog Performance Enhancement



System Level Techniques For Analog Performance Enhancement

Michiel Steyaert, Arthur van Roermund, Andrea Baschirotto

System Level Techniques For Analog Performance Enhancement:

System-level Techniques for Analog Performance Enhancement Bang-Sup Song, 2016-04-13 This book shows readers to avoid common mistakes in circuit design and presents classic circuit concepts and design approaches from the transistor to the system levels. The discussion is geared to be accessible and optimized for practical designers who want to learn to create circuits without simulations Topic by topic the author guides designers to learn the classic analog design skills by understanding the basic electronics principles correctly and further prepares them to feel confident in designing high performance state of the art CMOS analog systems This book combines and presents all in depth necessary information to perform various design tasks so that readers can grasp essential material without reading through the entire book This top down approach helps readers to build practical design expertise quickly starting from their understanding of electronics fundamentals Analog Circuit Design Michiel Steyaert, Arthur van Roermund, Andrea Baschirotto, 2011-09-15 Analog Circuit Design contains the contribution of 18 tutorials of the 20th workshop on Advances in Analog Circuit Design Each part discusses a specific to date topic on new and valuable design ideas in the area of analog circuit design Each part is presented by six experts in that field and state of the art information is shared and overviewed This book is number 20 in this successful series of Analog Circuit Design providing valuable information and excellent overviews of Topic 1 Low Voltage Low Power chairman Andrea Baschirotto Topic 2 Short Range Wireless Front Ends chairman Arthur van Roermund Topic 3 Power Management and DC DC chairman Michiel Stevaert Analog Circuit Design is an essential reference source for analog circuit designers and researchers wishing to keep abreast with the latest development in the field The tutorial coverage also makes it suitable for use in an advanced design course Stochastic Process Variation in Deep-Submicron CMOS Amir Ziaio.2013-11-19 One of the most notable features of nanometer scale CMOS technology is the increasing magnitude of variability of the key device parameters affecting performance of integrated circuits The growth of variability can be attributed to multiple factors including the difficulty of manufacturing control the emergence of new systematic variation generating mechanisms and most importantly the increase in atomic scale randomness where device operation must be described as a stochastic process In addition to wide sense stationary stochastic device variability and temperature variation existence of non stationary stochastic electrical noise associated with fundamental processes in integrated circuit devices represents an elementary limit on the performance of electronic circuits In an attempt to address these issues Stochastic Process Variation in Deep Submicron CMOS Circuits and Algorithms offers unique combination of mathematical treatment of random process variation electrical noise and temperature and necessary circuit realizations for on chip monitoring and performance calibration The associated problems are addressed at various abstraction levels i e circuit level architecture level and system level It therefore provides a broad view on the various solutions that have to be used and their possible combination in very effective complementary techniques for both analog mixed signal and digital circuits The feasibility of

the described algorithms and built in circuitry has been verified by measurements from the silicon prototypes fabricated in standard 90 nm and 65 nm CMOS technology Digital Subsampling Phase Lock Techniques for Frequency Synthesis and Polar Transmission Nereo Markulic, Kuba Raczkowski, Jan Craninckx, Piet Wambacq, 2019-01-30 This book explains concepts behind fractional subsampling based frequency synthesis that is re shaping today s art in the field of low noise LO generation It covers advanced material giving clear guidance for development of background calibrated environments capable of spur free synthesis and wideband phase modulation It further expands the concepts into the field of subsampling polar transmission where the newly developed architecture enables unprecedented spectral efficiency levels unquestionably required by the upcoming generation of wireless standards **Low-power HF Microelectronics** Gerson A. S. Machado, 1996 This book brings together innovative modelling simulation and design techniques in CMOS SOI GaAs and BJT to achieve successful high yield manufacture for low power high speed and reliable by design analogue and mixed mode Ofdm Based Relay Systems for Future Wireless Communications Milica Pejanovic-Djurisic, Enis integrated systems Kocan, Ramjee Prasad, 2022-09-01 Relay systems have become a subject of intensive research interest over the recent years as it is recognized that they can improve performances and extend the coverage area of wireless communication systems Special attention has been dedicated to them since the proposal appeared for their implementation in mobile cellular systems Numerous researches conducted after that proposal have enabled incorporation of OFDM based relay systems in both accepted standards for IMT Advanced systems Nowadays researches are ongoing with the aim to define new solutions for performance improvement of the standardized OFDM relay systems for cellular networks and one of the interesting solutions is implementation of subcarrier permutation SCP at the relay R station The book OFDM based relay systems for future wireless communications presents a comprehensive research results in analyzing behavior and performance of the OFDM based relay systems with SCP Dual hop relay scenario with three communication terminals and no direct link between the source S and the destination D has been analyzed as it is compliant with the accepted solutions for IMT Advanced systems The book includes performance analysis and performance comparison of OFDM based amplify and forward AF relay systems with fixed gain FG amplify and forward AF relay systems with variable gain VG decode and forward DF relay systems each including two SCP schemes known to maximize the system capacity and or improve the bit error rate BER performances Performance comparisons have enabled definition of optimal solutions for the future wireless communication systems in a given conditions and for the given optimality criteria OFDM based relay systems for future wireless communications contains recent research results in this area and is ideal for the academic staff and master research students in area of mobile communication systems as well as for the personnel in communication industry Smart and Flexible Digital-to-Analog Converters Georgi Radulov, Patrick Quinn, Hans Hegt, Arthur H.M. van Roermund, 2011-01-07 Smart and Flexible Digital to Analog Converters proposes new concepts and implementations for flexibility and self correction of current steering digital to

analog converters DACs which allow the attainment of a wide range of functional and performance specifications with a much reduced dependence on the fabrication process DAC linearity is analysed with respect to the accuracy of the DAC unit elements A classification is proposed of the many different current steering DAC correction methods The classification reveals methods that do not yet exist in the open literature Further this book systematically analyses self calibration correction methods for the various DAC mismatch errors For instance efficient calibration of DAC binary currents is identified as an important missing method This book goes on to propose a new methodology for correcting mismatch errors of both nominally identical unary as well as scaled binary DAC currents A new concept for DAC flexibility is presented The associated architecture is based on a modular design approach that uses parallel sub DAC units to realize flexible design functionality and performance Two main concepts self calibration and flexibility are demonstrated in practice using three DAC testchips in 250nm 180nm and 40nm standard CMOS Smart and Flexible Digital to Analog Converters will be useful to both advanced professionals and newcomers in the field Advanced professionals will find new methods that are fully elaborated from analysis at conceptual level to measurement results at test chip level New comers in the field will find structured knowledge of fully referenced state of the art methods with many fully explained novelties p DAC linearity is analysed with respect to the accuracy of the DAC unit elements A classification is proposed of the many different current steering DAC correction methods The classification reveals methods that do not yet exist in the open literature Further this book systematically analyses self calibration correction methods for the various DAC mismatch errors For instance efficient calibration of DAC binary currents is identified as an important missing method This book goes on to propose a new methodology for correcting mismatch errors of both nominally identical unary as well as scaled binary DAC currents A new concept for DAC flexibility is presented The associated architecture is based on a modular design approach that uses parallel sub DAC units to realize flexible design functionality and performance Two main concepts self calibration and flexibility are demonstrated in practice using three DAC testchips in 250nm 180nm and 40nm standard CMOS Smart and Flexible Digital to Analog Converters will be useful to both advanced professionals and newcomers in the field Advanced professionals will find new methods that are fully elaborated from analysis at conceptual level to measurement results at test chip level New comers in the field will find structured knowledge of fully referenced state of the art methods with many fully explained novelties This book goes on to propose a new methodology for correcting mismatch errors of both nominally identical unary as well as scaled binary DAC currents A new concept for DAC flexibility is presented The associated architecture is based on a modular design approach that uses parallel sub DAC units to realize flexible design functionality and performance Two main concepts self calibration and flexibility are demonstrated in practice using three DAC testchips in 250nm 180nm and 40nm standard CMOS Smart and Flexible Digital to Analog Converters will be useful to both advanced professionals and newcomers in the field Advanced professionals will find new methods that are fully elaborated from analysis at conceptual

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