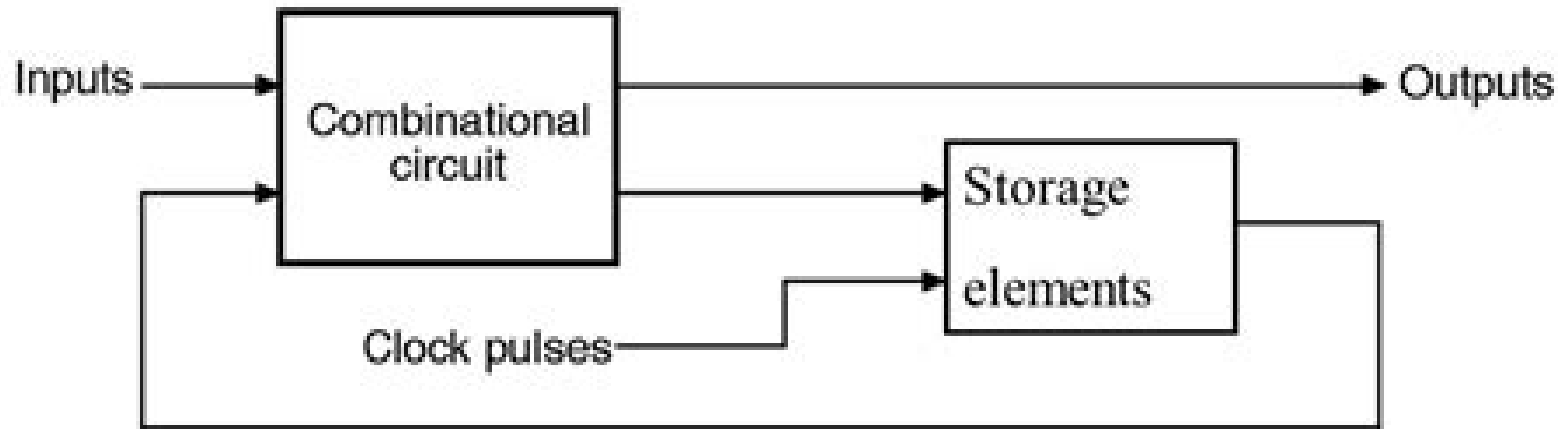
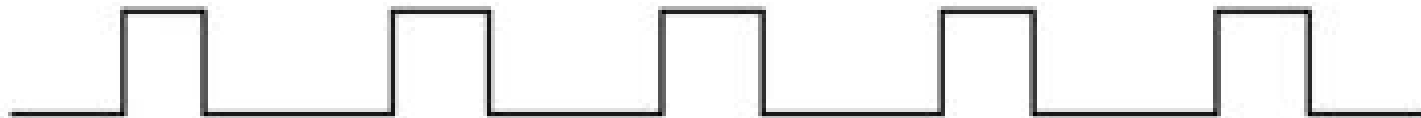


Synchronous Sequential Logic Circuit

- A synchronous sequential circuit, by definition, must employ signals that affect the memory elements only at discrete instants of time.



(a) Block diagram



(b) Timing diagram of clock pulses

Synchronous Precharge Logic Synchronous Precharge Logic

**Kerry Bernstein, K.M.
Carrig, Christopher M. Durham, Patrick
R. Hansen, David Hogenmiller, Edward
J. Nowak, Norman J. Rohrer**

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Asynchronous Pulse Logic Mika M. Nystrom, Alain Martin, 2007-05-08 Asynchronous Pulse Logic is a comprehensive analysis of a newly developed asynchronous circuit family The book covers circuit theory practical circuits design tools and an example of the design of a simple asynchronous microprocessor using the circuit family Asynchronous Pulse Logic will be of interest to industrial and academic researcher working on high speed VLSI systems Graduate students will find this useful reference for computer aided design of asynchronous or related VLSI systems

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Circuit Design for CMOS VLSI John P. Uyemura, 2012-12-06 During the last decade CMOS has become increasingly attractive as a basic integrated circuit technology due to its low power at moderate frequencies good scalability and rail to rail operation There are now a variety of CMOS circuit styles some based on static complementary conductance properties but others borrowing from earlier NMOS techniques and the advantages of using clocking disciplines for precharge evaluate sequencing In this comprehensive book the reader is led systematically through the entire range of CMOS circuit design Starting with the individual MOSFET basic circuit building blocks are described leading to a broad view of both combinatorial and sequential circuits Once these circuits are considered in the light of CMOS process technologies important topics in circuit performance are considered including characteristics of interconnect gate delay device sizing and I O

buffering Basic circuits are then composed to form macro elements such as multipliers where the reader acquires a unified view of architectural performance through parallelism and circuit performance through careful attention to circuit level and layout design optimization Topics in analog circuit design reflect the growing tendency for both analog and digital circuit forms to be combined on the same chip and a careful treatment of BiCMOS forms introduces the reader to the combination of both FET and bipolar technologies on the same chip to provide improved performance

High Speed CMOS Design

Styles Kerry Bernstein, K.M. Carrig, Christopher M. Durham, Patrick R. Hansen, David Hogenmiller, Edward J. Nowak, Norman J. Rohrer, 2012-12-06 High Speed CMOS Design Styles is written for the graduate level student or practicing engineer who is primarily interested in circuit design It is intended to provide practical reference or horse sense to mechanisms typically described with a more academic slant This book is organized so that it can be used as a textbook or as a reference book High Speed CMOS Design Styles provides a survey of design styles in use in industry specifically in the high speed microprocessor design community Logic circuit structures I/O and interface clocking and timing schemes are reviewed and described Characteristics sensitivities and idiosyncrasies of each are highlighted High Speed CMOS Design Styles also pulls together and explains contributors to performance variability that are associated with process applications conditions and design Rules of thumb and practical references are offered Each of the general circuit families is then analyzed for its sensitivity and response to this variability High Speed CMOS Design Styles is an excellent source of ideas and a compilation of observations that highlight how different approaches trade off critical parameters in design and process space

Microelectronics, II.

, 1983 **Asynchronous Circuit Design for VLSI Signal Processing** Teresa H. Meng, Sharad Malik, 2011-06-27

Asynchronous Circuit Design for VLSI Signal Processing is a collection of research papers on recent advances in the area of specification design and analysis of asynchronous circuits and systems This interest in designing digital computing systems without a global clock is prompted by the ever growing difficulty in adopting global synchronization as the only efficient means to system timing Asynchronous circuits and systems have long held interest for circuit designers and researchers alike because of the inherent challenge involved in designing these circuits as well as developing design techniques for them The frontier research in this area can be traced back to Huffman's publications The Synthesis of Sequential Switching Circuits in 1954 followed by Unger's book Asynchronous Sequential Switching Circuits in 1969 where a theoretical foundation for handling logic hazards was established In the last few years a growing number of researchers have joined force in unveiling the mystery of designing correct asynchronous circuits and better yet have produced several alternatives in automatic synthesis and verification of such circuits This collection of research papers represents a balanced view of current research efforts in the design synthesis and verification of asynchronous systems

Security Trends for FPGAs

Benoit Badrignans, Jean Luc Danger, Viktor Fischer, Guy Gogniat, Lionel Torres, 2011-06-20 In Security Trends for FPGAs the authors present an analysis of current threats against embedded systems and especially FPGAs They discuss about requirements

according to the FIPS standard in order to build a secure system This point is of paramount importance as it guarantees the level of security of a system Also highlighted are current vulnerabilities of FPGAs at all the levels of the security pyramid It is essential from a design point of view to be aware of all the levels in order to provide a comprehensive solution The strength of a system is defined by its weakest point there is no reason to enhance other protection means if the weakest point remains untreated Many severe attacks have considered this weakness in order not to face brute force attack complexity Several solutions are proposed in Security Trends for FPGA s especially at the logical architecture and system levels in order to provide a global solution

Synchronization Design for Digital Systems Teresa H. Meng, 2012-12-06 Synchronization is one of the important issues in digital system design While other approaches have always been intriguing up until now synchro nous operation using a common clock has been the dominant design philo sophy However we have reached the point with advances in technology where other options should be given serious consideration This is because the clock periods are getting much smaller in relation to the interconnect propagation delays even within a single chip and certainly at the board and backplane level To a large extent this problem can be overcome with care ful clock distribution in synchronous design and tools for computer aided design of clock distribution However this places global constraints on the design making it necessary for example to redesign the clock distribution each time any part of the system is changed In this book some alternative approaches to synchronization in digital sys tem design are described and developed We owe these techniques to a long history of effort in both digital system design and in digital communica tions the latter field being relevant because large propagation delays have always been a dominant consideration in design While synchronous design is discussed and contrasted to the other techniques in Chapter 6 the dom inant theme of this book is alternative approaches

Seventeenth Conference on Advanced Research in VLSI Richard B. Brown, Alexander T. Ishii, 1997 This volume on computational intelligence covers the 17th Conference on Advanced Research in VLSI in 1997 Topics include VLSI architecture asynchronous design circuits layout image sensors optimization system timing CAD and low power design

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