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Smart Power ICs Bruno Murari, 2002-06-13 This book provides a survey of the state of the art of technology and future trends in the new family of Smart Power ICs and describes design and applications in a variety of fields ranging from automotive to telecommunications reliability evaluation and qualification procedures The book is a valuable source of information and reference for both power IC design specialists and to all those concerned with applications the development of digital circuits and with system architecture

High-Frequency Bipolar Transistors Michael Reisch, 2003-03-05 This modern book length treatment gives a detailed presentation of high frequency bipolar transistors in silicon or silicon germanium technology with particular emphasis placed on today s advanced compact models and their physical foundations

High Dielectric Constant Materials Howard Huff, David Gilmer, 2005-11-02 Issues relating to the high K gate dielectric are among the greatest challenges for the evolving International Technology Roadmap for Semiconductors ITRS More than just an historical overview this book will assess previous and present approaches related to scaling the gate dielectric and their impact along with the creative directions and forthcoming challenges that will define the future of gate dielectric scaling technology Topics include an extensive review of Moore s Law the classical regime for SiO₂ gate dielectrics the transition to silicon oxynitride gate dielectrics the transition to high K gate dielectrics including the drive towards equivalent oxide thickness in the single digit nanometer regime and future directions and issues for ultimate technology generation scaling The vision wisdom and experience of the team of authors will make this book a timely relevant and interesting resource focusing on fundamentals of the 45 nm Technology Generation and beyond

Integrated CMOS Circuits for Optical Communications Mark Ingels, Michiel Steyaert, 2013-03-09 This work investigates the feasibility of the integration of interface circuits for optical communication systems in a standard unmodified digital CMOS process This paves the way for single chip communication systems where the optical interfaces are integrated on the same die as the required digital circuitry The optical receiver is a key element in the optical communication link In this work a transimpedance amplifier which consists of a voltage amplifier with resistive feedback is used as the first stage Unlike for many other circuits the optimal place of its dominant pole is the input node It is also demonstrated that a high gain of the voltage amplifier is primordial to obtain good performances and that this may be obtained through the use of multiple stages Noise aspects are investigated and the conclusion is drawn that the amplifier s input capacitance can be smaller than the photodiode s capacitance for optimal performance

The ESD Handbook Steven H. Voldman, 2021-04-12 A practical and comprehensive reference that explores Electrostatic Discharge ESD in semiconductor components and electronic systems The ESD Handbook offers a comprehensive reference that explores topics relevant to ESD design in semiconductor components and explores ESD in various systems Electrostatic discharge is a common problem in the semiconductor environment and this reference fills a gap in the literature by discussing ESD protection Written by a noted expert on the topic the text offers a topic by topic reference

that includes illustrative figures discussions and drawings The handbook covers a wide range of topics including ESD in manufacturing garments wrist straps and shoes ESD Testing ESD device physics ESD semiconductor process effects ESD failure mechanisms ESD circuits in different technologies CMOS Bipolar etc ESD circuit types Pin Power Pin to Pin etc and much more In addition the text includes a glossary index tables illustrations and a variety of case studies Contains a well organized reference that provides a quick review on a range of ESD topics Fills the gap in the current literature by providing information from purely scientific and physical aspects to practical applications Offers information in clear and accessible terms Written by the accomplished author of the popular ESD book series Written for technicians operators engineers circuit designers and failure analysis engineers The ESD Handbook contains an accessible reference to ESD design and ESD systems

ESD Steven H. Voldman, 2009-07-01 Electrostatic discharge ESD failure mechanisms continue to impact semiconductor components and systems as technologies scale from micro to nano electronics This book studies electrical overstress ESD and latchup from a failure analysis and case study approach It provides a clear insight into the physics of failure from a generalist perspective followed by investigation of failure mechanisms in specific technologies circuits and systems The book is unique in covering both the failure mechanism and the practical solutions to fix the problem from either a technology or circuit methodology Look inside for extensive coverage on failure analysis tools EOS and ESD failure sources and failure models of semiconductor technology and how to use failure analysis to design more robust semiconductor components and systems electro thermal models and technologies the state of the art technologies discussed include CMOS BiCMOS silicon on insulator SOI bipolar technology high voltage CMOS HVCMOS RF CMOS smart power gallium arsenide GaAs gallium nitride GaN magneto resistive MR giant magneto resistors GMR tunneling magneto resistor TMR devices micro electro mechanical MEM systems and photo masks and reticles practical methods to use failure analysis for the understanding of ESD circuit operation temperature analysis power distribution ground rule development internal bus distribution current path analysis quality metrics connecting the theoretical to the practical analysis the failure of each key element of a technology from passives active elements to the circuit sub system to package highlighted by case studies of the elements circuits and system on chip SOC in today's products ESD Failure Mechanisms and Models is a continuation of the author's series of books on ESD protection It is an essential reference and a useful insight into the issues that confront modern technology as we enter the Nano electronic era

Silicon Optoelectronic Integrated Circuits Horst Zimmermann, 2013-03-09 Explains the circuit design of silicon optoelectronic integrated circuits OEICs which are central to advances in wireless and wired telecommunications The essential features of optical absorption are summarized as is the device physics of photodetectors and their integration in modern bipolar CMOS and BiCMOS technologies This information provides the basis for understanding the underlying mechanisms of the OEICs described in the main part of the book In order to cover the topic comprehensively Silicon Optoelectronic Integrated Circuits presents detailed descriptions of many OEICs

for a wide variety of applications from various optical sensors smart sensors 3D cameras and optical storage systems DVD to fiber receivers in deep sub m CMOS Numerous detailed illustrations help to elucidate the material

System-level Test and Validation of Hardware/Software Systems Matteo Sonza Reorda,Zebo Peng,Massimo Violante,2006-03-30 New manufacturing technologies have made possible the integration of entire systems on a single chip This new design paradigm termed system on chip SOC together with its associated manufacturing problems represents a real challenge for designers SOC is also reshaping approaches to test and validation activities These are beginning to migrate from the traditional register transfer or gate levels of abstraction to the system level Until now test and validation have not been supported by system level design tools so designers have lacked the infrastructure to exploit all the benefits stemming from the adoption of the system level of abstraction Research efforts are already addressing this issue This monograph provides a state of the art overview of the current validation and test techniques by covering all aspects of the subject including modeling of bugs and defects stimulus generation for validation and test purposes including timing errors design for testability

Current Sense Amplifiers for Embedded SRAM in High-Performance System-on-a-Chip Designs Bernhard Wicht,2013-04-17 System on a chip SoC designs result in a wide range of high complexity high value semiconductor products As the technology scales towards smaller feature sizes and chips grow larger a speed limitation arises due to an increased RC delay associated with interconnection wires Innovative circuit techniques are required to achieve the speed needed for high performance signal processing Current sensing is considered as a promising circuit class since it is inherently faster than conventional voltage sense amplifiers However especially in SRAM current sensing has rarely been used so far Practical implementations are challenging because they require sophisticated analog circuit techniques in a digital environment The objective of this book is to provide a systematic and comprehensive insight into current sensing techniques Both theoretical and practical aspects are covered Design guidelines are derived by systematic analysis of different circuit principles Innovative concepts like compensation of the bit line multiplexer and auto power down will be explained based on theory and experimental results The material will be interesting for design engineers in industry as well as researchers who want to learn about and apply current sensing techniques The focus is on embedded SRAM but the material presented can be adapted to single chip SRAM and to any other current providing memory type as well This includes emerging memory technologies like magnetic RAM MRAM and Ovonic Unified Memory OUM Moreover it is also applicable to array like structures such as CMOS camera chips and to circuits for signal transmission along highly capacitive busses

Lock-in Thermography Otwin Breitenstein,Wilhelm Warta,Martin Langenkamp,2013-03-09 Although the first publication on lock in thermography appeared in 1988 concerning electronic device testing this technique only became popular in the 1990s in connection with the nondestructive testing of materials NDT especially photothermal and thermoelastic investigations In the early 1990s our group at the Max Planck Institute of Microstructure Physics in Halle had the task to image small leakage currents in silicon

solar cells We soon realized that neither conventional steady state thermography nor the only available lock in thermography system of that time was sensitive enough to image the tiny temperature differences caused by these leakage currents Therefore we developed the Dynamic Precision Contact Thermography technique DPCT which was the first lock in thermography system having a detection limit below 100 μ K However this system turned out to be too impractical for general use since it worked in a mechanical contacting mode and its measurement time was necessarily many hours With the availability of highly sensitive focal plane array thermocameras at the end of the 1990s the way was opened to construct highly sensitive IR based lock in thermography systems This was done independently by groups working in NDT and by us working in electronic device testing whereby the different demands in the different fields lead to partly different approaches in the realization For photothermal investigations a low lock in frequency is usually used in order to see sub surface details and for thermoelastic investigations the thermocamera cannot usually be synchronized to the temperature modulation

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